WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of semiconductor chips having a plurality of terminals;

two chip mounting bases on each of which at least one of the semiconductor chips is mounted and a plurality of chip interconnections electrically connected to the terminals of the mounted semiconductor chip are formed into substantially the same pattern and which are stacked in two layers along a direction of thickness;

one interconnection base which is interposed between the two chip mounting bases and on which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from the pattern of the chip interconnections; and

a plurality of interlevel interconnections which are formed in a plurality of through holes extending through the chip mounting bases and the interconnection base at once along a stacking direction and electrically connect the chip interconnections and the intermediate interconnections in the stacking direction of the bases.

2. A device according to claim 1, wherein:

the chip interconnections and the intermediate interconnections are formed on facing major surfaces of

at least one of the two chip mounting bases and the interconnection base.

3. A device according to claim 1, wherein:

the through holes extend through feedthrough terminals of the chip interconnections and the intermediate interconnections.

4. A device according to claim 1, wherein:

the intermediate interconnections are formed into a pattern capable of setting signal paths from the terminals independently for each terminal and each layer.

5. A device according to claim 4, wherein:

the intermediate interconnections are formed into a pattern capable of switching, between the layers for each terminal, signal paths between the terminals and a plurality of external terminals which externally electrically connect the semiconductor chips.

6. A semiconductor device comprising:

a plurality of semiconductor chips having a plurality of terminals;

two chip mounting bases on each of which at least one of the semiconductor chips is mounted and a plurality of chip interconnections electrically connected to the terminals of the mounted semiconductor chip are formed into substantially the same pattern and which are stacked in two layers along a direction of thickness;

a first interconnection base which is interposed between the two chip mounting bases and on which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from the pattern of the chip interconnections;

a second interconnection base which is arranged together with the first interconnection base alternately with the chip mounting bases and on which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from the pattern of the chip interconnections and the pattern of the intermediate interconnections formed on the first interconnection base; and

a plurality of interlevel interconnections which are formed in a plurality of through holes extending through the chip mounting bases, the first interconnection base, and the second interconnection base at once along a stacking direction and electrically connect the chip interconnections and the intermediate interconnections in the stacking direction of the bases.

7. A device according to claim 6, wherein:

the chip interconnections and the intermediate interconnections are formed on facing major surfaces of the bases for a pair of at least one of the two chip

mounting bases and the first or second interconnection base adjacent to the chip mounting base.

8. A device according to claim 6, wherein:

the chip interconnections and the intermediate interconnections are formed on facing major surfaces of the bases for a pair of one of the two chip mounting bases and the first interconnection base and a pair of the other chip mounting base and the second interconnection base.

9. A device according to claim 6, wherein:

the through holes extend through feedthrough terminals of the chip interconnections and the intermediate interconnections.

10. A device according to claim 6, wherein:

the intermediate interconnections are formed into a pattern capable of setting signal paths from the terminals independently for each terminal and each layer.

11. A device according to claim 10, wherein:

the intermediate interconnections are formed into a pattern capable of switching, between the layers for each terminal, signal paths between the terminals and a plurality of external terminals which externally electrically connect the semiconductor chips.

12. A semiconductor device comprising:

a plurality of semiconductor chips having a plurality of terminals;

a plurality of chip mounting bases on each of which at least one of the semiconductor chips is mounted and which are stacked in a plurality of layers along a direction of thickness;

a plurality of chip interconnections which are formed into substantially the same pattern on the chip mounting bases and electrically connected to the terminals of the semiconductor chips mounted on the chip mounting bases;

a plurality of interconnection bases which are arranged alternately with the chip mounting bases along a stacking direction of the chip mounting bases;

a plurality of intermediate interconnections which are formed into predetermined patterns for the respective interconnection bases that are different from the pattern of the chip interconnections, and electrically connected to the chip interconnections; and

a plurality of interlevel interconnections which are formed in a plurality of through holes extending through the chip mounting bases and the interconnection bases at once along the stacking direction and electrically connect the chip interconnections and the intermediate interconnections in the stacking direction of the bases.

13. A device according to claim 12, wherein:

the chip interconnections and the intermediate

interconnections are formed on facing major surfaces of the bases for a pair of a chip mounting base in at least one predetermined layer among the chip mounting bases and at least one interconnection base adjacent to the chip mounting base.

14. A device according to claim 12, wherein:

the number of interconnection bases equal to the number of chip mounting bases are arranged, and the chip interconnections and the intermediate interconnections are formed on facing major surfaces of the bases for all pairs of the chip mounting bases and the interconnection bases adjacent to the chip mounting bases.

15. A device according to claim 12, wherein:

the through holes extend through feedthrough terminals of the chip interconnections and the intermediate interconnections.

16. A device according to claim 12, wherein:

the intermediate interconnections are formed into a pattern capable of setting signal paths from the terminals independently for each terminal and each layer.

17. A device according to claim 16, wherein:

the intermediate interconnections are formed into a pattern capable of switching, between the layers for each terminal, signal paths between the terminals and a plurality of external terminals which externally

electrically connect the semiconductor chips.

18. A semiconductor device manufacturing method comprising:

stacking, in two layers along a direction of thickness, two chip mounting bases on each of which a plurality of chip interconnections electrically connected to a plurality of terminals of semiconductor chips are formed into substantially the same pattern and at least one of the semiconductor chips is mounted by electrically connecting the terminals to the chip interconnections;

interposing, between the chip mounting bases, one interconnection base on which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from the pattern of the chip interconnections; and

forming a plurality of through holes through the chip mounting bases and the interconnection base at once along a stacking direction, and forming, in the through holes, a plurality of interlevel interconnections which electrically connect the chip interconnections and the intermediate interconnections in the stacking direction of the bases.

19. A method according to claim 18, wherein:

for at least one of the two chip mounting bases and the interconnection base, a major surface of the

chip mounting base on which the chip interconnections are formed and a major surface of the interconnection base on which the intermediate interconnections are formed are arranged to face each other.

20. A method according to claim 18, wherein:

the through holes are formed after integrating the chip mounting bases and the interconnection base.

21. A method according to claim 18, wherein:

the through holes are formed through feedthrough terminals of the chip interconnections and the intermediate interconnections.

22. A semiconductor device manufacturing method comprising:

stacking, in two layers along a direction of thickness, two chip mounting bases on each of which a plurality of chip interconnections electrically connected to a plurality of terminals of semiconductor chips are formed into substantially the same pattern and at least one of the semiconductor chips is mounted by electrically connecting the terminals to the chip interconnections;

interposing, between the chip mounting bases, a first interconnection base on which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from the pattern of the chip interconnections;

arranging, together with the first interconnection base alternately with the chip mounting bases, a second interconnection base on which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from the pattern of the chip interconnections and the pattern of the intermediate interconnections formed on the first interconnection base; and

forming a plurality of through holes through the chip mounting bases, the first interconnection base, and the second interconnection base at once along a stacking direction, and forming, in the through holes, a plurality of interlevel interconnections which electrically connect the chip interconnections and the intermediate interconnections in the stacking direction of the bases.

23. A method according to claim 22, wherein:

for a pair of at least one of the two chip mounting bases and the first or second interconnection base adjacent to the chip mounting base, a major surface of the chip mounting base on which the chip interconnections are formed and a major surface of the first or second interconnection base on which the intermediate interconnections are formed are arranged to face each other.

24. A method according to claim 22, wherein:

for a pair of one of the two chip mounting bases

and the first interconnection base and a pair of the other chip mounting base and the second interconnection base, major surfaces of the chip mounting bases on which the chip interconnections are formed and major surfaces of the first and second interconnection bases on which the intermediate interconnections are formed are arranged to face each other.

25. A method according to claim 22, wherein:

the through holes are formed after integrating the chip mounting bases, the first interconnection base, and the second interconnection base.

26. A method according to claim 22, wherein:

the through holes are formed through feedthrough terminals of the chip interconnections and the intermediate interconnections.

27. A semiconductor device manufacturing method comprising:

stacking, in a plurality of layers along a direction of thickness, a plurality of chip mounting bases on each of which a plurality of chip interconnections electrically connected to a plurality of terminals of semiconductor chips are formed into substantially the same pattern and at least one of the semiconductor chips is mounted by electrically connecting the terminals to the chip interconnections;

arranging, alternately with the chip mounting bases along a stacking direction of the chip mounting

bases, a plurality of interconnection bases on each of which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into predetermined patterns different from the pattern of the chip interconnections; and

forming a plurality of through holes through the chip mounting bases and the interconnection bases at once along the stacking direction, and forming, in the through holes, a plurality of interlevel interconnections which electrically connect the chip interconnections and the intermediate interconnections in the stacking direction of the bases.

28. A method according to claim 27, wherein:

for a pair of a chip mounting base in at least one predetermined layer among the chip mounting bases and at least one interconnection base adjacent to the chip mounting base, a major surface of the chip mounting base on which the chip interconnections are formed and a major surface of the interconnection base on which the intermediate interconnections are formed are arranged to face each other.

29. A method according to claim 27, wherein:

the number of interconnection bases equal to the number of chip mounting bases are arranged, and for all pairs of the chip mounting bases and the interconnection bases adjacent to the chip mounting bases, major surfaces of the chip mounting bases on

which the chip interconnections are formed and major surfaces of the interconnection bases on which the intermediate interconnections are formed are arranged to face each other.

30. A method according to claim 27, wherein:

the through holes are formed after integrating the chip mounting bases and the interconnection bases.

31. A method according to claim 27, wherein:

the through holes are formed through feedthrough terminals of the chip interconnections and the intermediate interconnections.